Please amend the above-identified application as follows:

IN THE CLAIMS:

1. (Currently Amended) A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit operable to store blocks of media data and to output a first block of media data to be processed;

a second memory unit operable to store blocks of media data and to output a second block of media data to be processed;

a first multiplexer coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a selected one of the first block of media data and the second block of media data;

a combiner coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a combined block of media data corresponding to a portion of the first block of media data and a portion of the second block of media data;

a second multiplexer coupled to the output of the first multiplexer and the output of the combiner and operable to output a selected one of the combined block of media data and the selected one of the first block of media data and the second block of media data; and

a single instruction, multiple data (SIMD) processor operable to receive blocks of

media data from the second multiplexer ~~first and second memory units~~ and to perform filtering operations on blocks of media data from the first and second memory units concurrently;

~~wherein the SIMD processor is operable to retrieve less than all bits stored in a first memory location in the first memory unit and less than all bits stored in a second memory location in the second memory unit, and wherein the SIMD processor is operable to concurrently perform filtering operations on the bits from the first memory location and the bits from the second memory location~~.

2. (Currently Amended) The filter engine of claim 1 wherein the SIMD processor is adapted to receive the selected one of the first block of media data and the second block of media data from the second multiplexer ~~blocks of data from the first and second memory units, and to concurrently perform filtering operations on blocks of data from the first and second memory units,~~ when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the SIMD processor is adapted to receive the combined block of media data from the second multiplexer ~~blocks of data from only one of the first and second memory units, and to perform filtering operations on the received blocks of data~~.

3-4. (Canceled)

5. (Currently Amended) The filter engine of claim 1 wherein the SIMD processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and ~~wherein~~ when the filter engine is in a split-operation mode, the first set of data path units is adapted to perform filtering operations on [[a]] the first block of media data received from the first memory unit while the second set of data path units is concurrently performing filtering operations on [[a]] the second block of media data received from the second memory unit.

6. (Currently Amended) The filter engine of claim [[5]] 1 wherein the SIMD processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and ~~wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first memory unit while the second set of data path units concurrently performs filtering operations on a block of data received from the second memory unit, and wherein~~ when the filter engine is in a non-split operation mode, both the first and second sets of data path units perform filter operations on the combined block of media data ~~blocks of data from only one of the first and second memory units~~.

7-8. (Canceled)

9. (Previously Presented) The filter engine of claim 1 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein:

the first memory unit is adapted to store blocks of pixel data to be processed;

the second memory unit is adapted to store blocks of pixel data to be processed; and

the SIMD processor is adapted to receive blocks of pixel data from the first and second memory units and to perform filtering operations on blocks of pixel data from the first and second memory units concurrently.

10. (Currently Amended) A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of video data, the filter engine comprising:

a first memory unit operable to store blocks of video data and to output a first block of video data to be processed;

a second memory unit operable to store blocks of video data and to output a second block of video data to be processed;

a combiner coupled to the output of the first memory unit and to the output of the second memory unit and operable to output a combined block of video data corresponding to a portion of the first block of video data and a portion of the second block of video data;

a first shift register operable to receive and store a selected one of the first block of video data and the combined block of video data ~~blocks of video data from the first memory unit, wherein the first shift register is adapted to selectively shift its contents by~~

~~a predetermined number of bits corresponding to the number of bits used to represent one pixel, said shift requiring only a single clock cycle~~;

a second shift register operable to receive and store the second block of video data ~~blocks of video data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to the number of bits used to represent one pixel, said shift requiring only a single clock cycle~~; and

a processor operable to receive blocks of video data from the first and second shift registers and to perform filtering operations on blocks of video data from the first and second shift registers concurrently.

11. (Canceled)

12. (Currently Amended) The filter engine of claim 10 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to concurrently perform filtering operations on blocks of video data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of video data from ~~one of~~ the first and second memory units, and the processor is adapted to receive blocks of video data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of video data from the first shift register.

13. (Previously Presented) The filter engine of claim 12 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor concurrently performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

14. (Previously Presented) The filter engine of claim 13 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of concurrently performing filtering operations on.

15. (Currently Amended) The filter engine of claim 10 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of video data received from the first shift register while the second set of data path units is concurrently performing filtering operations on a block of video data received from the second shift register.

16. (Currently Amended) The filter engine of claim 15 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of video data received from the first shift register while the second set of data path units concurrently performs filtering operations on a block of video data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of video data from ~~one of~~ the first and second memory units, and both the first and second sets of data path units perform filter operations on blocks of video data from the first shift register, but not from the second shift register.

17. (Previously Presented) The filter engine of claim 16 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units concurrently performs filtering operations on then most significant bits of the second shift register.

18. (Previously Presented) The filter engine of claim 17 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of concurrently performing filtering operations on.

19-27. (Canceled)

28. (New) A system, comprising:

a first data storage means configured to output a first block of data;

a second data storage means configured to output a second block of data;

means for outputting a selected one of the first block of data and the second block of data;

means for outputting a combined block of data corresponding to a portion of the first block of data and a portion of the second block of data;

means for outputting a selected one of the combined block of data and the selected one of the first block of data and the second block of data; and

means for performing filtering operations on blocks of data from the first and second memory units concurrently.

29. (New) The system of claim 28, wherein the means for performing filtering operations is configured to receive the selected one of the first block of data and the second block of data when the system is in a split-operation mode, and wherein when the system is in a non-split-operation mode, the means for performing filtering operations is configured to receive the combined block of data.

30. (New) The system of claim 28, wherein the means for performing filtering operations comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and when the system is in a split-operation mode, the first set of data path units is configured to perform filtering operations on the first block of data while the second set of data path units is concurrently performing filtering operations on the second block of data.

31. (New) The system of claim 28, wherein the means for performing filtering operations comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and when the system is in a non-split operation mode, both the first and second sets of data path units are configured to perform filter operations on the combined block of data.

32. (New) The system of claim 28, wherein the first block of data and the second block of data correspond to pixel data.

33. (New) The system of claim 28, wherein the means for performing filtering operations comprises a plurality of data path units comprising a first set of data path units and a second set of data path units,

wherein when the system is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from a first shift register while the second set of data path units concurrently performs filtering operations on a block of data received from a second shift register, and

wherein when the system is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from the first data storage means and the second data storage means, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

34. (New) The filter engine of claim 10, wherein the first and second shift registers are configured to selectively shift their contents by a predetermined number of bits corresponding to the size of one pixel.

35. (New) The filter engine of claim 1, wherein the portion of the first block of media data includes the m most significant bits of the first block of media data, and the portion of the second block of media data includes the n most significant bits of the second block of media data.

36. (New) The filter engine of claim 35, wherein t is the total number of bits in each of the first block of media data and the second block of media data, and m and n equal t divided by 2.